REMARKS

Claims 1, 4-13, 15 and 18 are pending.

Claims 1, 6, and 15 are currently amended.

Support for the amendments to claims 1, 6, and 15 may be found in the specification, for example in paragraph [0039].

Rejection of Claims under 35 U.S.C. § 103

Claims 1, 4-13, 15 and 18 stand rejected.

Claims 1, 5-8, 10, and 12-13 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Kopsaftis, U.S. Patent No. 5,659,801 ("Kopsaftis"), in view of Torrey et al., U.S. Patent Appl. No. 2003/0084240 ("Torrey"). Applicants respectfully traverse this rejection.

As amended, independent claim 1, and generally independent claim 6 recite, inter alia, "said first LUN processes I/O commands, and said second LUN processes microcode update commands,...said first device obtaining a LUN address from each of said one or more commands, in response to said LUN address obtained from each of said one or more commands *being equal to said second LUN,* ***... directly overwriting said microcode in said memory using said LUN address assigned to said memory by processing each of said one or more commands, thereby updating said stored microcode in said first device,*** "(emphasis added).

In contrast, Kopsaftis teaches that the "second disk control command" travels the same route as the "first disk control command", which is to the "resident processor 106" and which is first received and verified and then subsequently is "stored in the non-volatile memory 108" (*Kopsaftis column 6, lines 34 through 47*). Thus, the Kopsaftis appears to teach a single LUN address.

The single LUN address is illustrated in greater detail in column 8, lines 63 through column 9, line 15 of Kopsaftis where the commands are directed to the "resident processor 106" which conducts the distribution of the information. The distribution of new microcode is discussed at column 10, line 41 through column 11 line 35, where the command "is detected as an initiator command in the disk drive 10, in the manner described in detail above." column 11, lines 1-5.

Applicants submit that Kopsaftis only teach the use of one SCSI LUN during the microcode update, and that consequently, Kopsaftis teaches away from Claim 1. Applicant submit that it is improper to combine references where the references teach away from their combination. *In re Grasselli*, 713 F.2d 731, 743, 218 USPQ 769, 779 (Fed. Cir. 1983).

Therefore, Applicants submit that the cited portions of Kopsaftis fails to teach, and actually teaches away from, "said first LUN processes I/O commands, and said second LUN processes microcode update commands,…said first device obtaining a LUN address from each of said one or more commands, in response to said LUN address obtained from each of said one or more commands *being equal to said second LUN,* ***… directly overwriting said microcode in said memory using said LUN address assigned to said memory by processing each of said one or more commands, thereby updating said stored microcode in said first device,*** "(emphasis added).

Torrey describes using different LUNs for the same library controller to designate the actions or queries the controller takes with respect to various library resources. For example, the cited portions of Torrey teach the use of "logical unit numbering to address different portions of the library" (Torrey, paragraph [0015]) and that if a "request is directed to only a portion or specific elements of the library, the library controller uses the SCSI LUN assigned to the storage elements, media and I/O elements involved to carry out the request..." (Torrey, paragraph [0020]). Applicant can find no instance where Torrey teaches that the library controller have one LUN address, while its memory has another LUN address as required by independent claim 1.

Applicants submit that the cited portions of Torrey fails to teach that in response to said LUN address obtained from each of said one or more commands *being equal to said second LUN,* ***… directly overwriting said microcode in said memory using said LUN address assigned to said memory by processing each of said one or more commands, thereby updating said stored microcode in said first device,*** "(emphasis added).

Therefore, the cited portions of Kopsaftis and Torrey, either alone or in combination, do not disclose that in response to said LUN address obtained from each of said one or more commands *being equal to said second LUN,* ***… directly overwriting said microcode in said memory using said LUN address assigned to said memory by processing each of said one or more commands, thereby updating said stored microcode in said first device,*** "(emphasis added).

Accordingly, Applicants submit that all of the claim limitations of independent claims 1 and 6 have not been shown by Kopsaftis and Torrey, alone or in combination as required by § 706.02 (j) of the MPEP. It follows then that a *prima facie* case of obviousness has not been met with respect to claims 1 and 6. Accordingly, Applicants respectfully submit that claims 1 and 6 are allowable for at least this reason over Kopsaftis and Torrey, either alone or in combination.

Claim 5 depends from independent claim 1 and are allowable for at least this reason. Claims 7-8, 10, and 12-13 depend from independent claim 6, and are allowable for at least this reason.

Claim 4 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Kopsaftis and Torrey in further view of Shirasawa et al., U.S. Patent Appl. No. 2002/0166027 ("Shirasawa").

In re claim 4, Applicants submit above that the combination of Kopsaftis and Torrey fail to teach or suggest all of Applicants claim limitations in, at least, independent claim 1. Accordingly, as claim 4 depends from claim 1, Applicant respectfully submit that all of the claim limitations of claim 4 have not been shown by Kopsaftis and Torrey

in view of Shirasawa, alone or in combination. Accordingly, Applicants respectfully submit that claim 4 is allowable for at least this reason over Kopsaftis, Torrey and Shirasawa, either alone or in combination.

Claim 9 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Kopsaftis and Torrey in further view of Pellegrino et al., U.S. Patent Appl. No. 2004/0225775 ("Pellegrino").

In re claim 9, Applicants submit above that the combination of Kopsaftis and Torrey fail to teach or suggest all of Applicants claim limitations in, at least, independent claim 6. Accordingly, as claim 9 depends from claim 6, Applicant respectfully submit that all of the claim limitations of claim 9 have not been shown by Kopsaftis and Torrey in view of Pellegrino, alone or in combination. Accordingly, Applicants respectfully submit that claim 9 is allowable for at least this reason over Kopsaftis, Torrey and Pellegrino, either alone or in combination.

Claim 11 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Kopsaftis and Torrey in further view of Abbott et al., U.S. Patent No. 6,205,093 ("Abbott").

In re claim 11, Applicants submit above that the combination of Kopsaftis and Torrey fail to teach or suggest all of Applicants claim limitations in, at least, independent claim 6. Accordingly, as claim 11 depends from claim 6, Applicant respectfully submit that all of the claim limitations of claim 11 have not been shown by Kopsaftis and Torrey in view of Abbott, alone or in combination. Accordingly, Applicants respectfully submit that claim 11 is allowable for at least this reason over Kopsaftis, Torrey and Abbott, either alone or in combination.

Claim 14 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Kopsaftis and Torrey in further view of Burton et al., U.S. Patent No. 6,393,535 ("Burton").

As amended, independent claim 15 recites, inter alia, "said first LUN processes I/O commands, and said second LUN processes microcode update commands,…said first

device obtaining a LUN address from each of said one or more commands, in response to said LUN address obtained from each of said one or more commands *being equal to said second LUN,* ***... directly overwriting said microcode in said memory using said LUN address assigned to said memory by processing each of said one or more commands, thereby updating said stored microcode in said first device,*** "(emphasis added).

For the reasons stated above, Applicants submit the cited portions of Kopsaftis and Torrey, either alone or in combination, do not disclose that in response to said LUN address obtained from each of said one or more commands *being equal to said second LUN,* ***... directly overwriting said microcode in said memory using said LUN address assigned to said memory by processing each of said one or more commands, thereby updating said stored microcode in said first device,*** "(emphasis added).

Furthermore, the Applicants submit that Kopsaftis only teach the use of one SCSI LUN during the microcode update, and as such, that Kopsaftis teaches away from Claim 1. Applicant submit that it is improper to combine references where the references teach away from their combination. *In re Grasselli*, 713 F.2d 731, 743, 218 USPQ 769, 779 (Fed. Cir. 1983). Finally, Applicant can find no instance where Torrey teaches that the library controller have one LUN address, while its memory has another LUN address as required by independent claim 1.

The Office Action states Burton "teaches an article of manufacture comprising a data storage medium tangibly embodying a program of machine-readable instruction executed by a processing apparatus to perform method steps" (*Office Action paragraph 27).*

The cited portion of Burton does not disclose that in response said LUN address obtained from each of said one or more commands *being equal to said second LUN,* ***... directly overwriting said microcode in said memory using said LUN address assigned to said memory by processing each of said one or more commands, thereby updating said stored microcode in said first device,*** "(emphasis added).

The cited portions of Kopsaftis, Torrey, and Burton either alone or in combination, do not disclose, that in response said LUN address obtained from each of said one or more commands *being equal to said second LUN,* ***… directly overwriting said microcode in said memory using said LUN address assigned to said memory by processing each of said one or more commands, thereby updating said stored microcode in said first device,*** "(emphasis added).

Accordingly, Applicants submit that all of the claim limitations of independent claim 15 have not been shown by Kopsaftis, Torrey, and Burton, alone or in combination as required by § 706.02 (j) of the MPEP. It follows then that a *prima facie* case of obviousness has not been met with respect to claim 15. Accordingly, Applicants respectfully submit that claim 15 is allowable for at least this reason over Kopsaftis, Torrey, and Burton either alone or in combination.

Claim 18 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Kopsaftis, Torrey, and Burton, in further view of Shirasawa.

In re claim 18, Applicants submit above that the combination of Kopsaftis, Torrey and Burton fail to teach or suggest all of Applicants claim limitations in, at least, independent claim 15. Accordingly, as claim 18 depends from claim 15, Applicant respectfully submit that all of the claim limitations of claim 18 have not been shown by Kopsaftis, Torrey, Burton and Shirasawa, alone or in combination as required by §706.02 (j) of the MPEP. It follows then that a *prima facie* case of obviousness has not been met with respect to claim 18. Accordingly, Applicants respectfully submit that claim 18 is allowable for at least this reason over Kopsaftis, Torrey, Burton and Shirasawa, either alone or in combination.

CONCLUSION

In view of the remarks set forth herein, the application is believed to be in condition for allowance and a notice to that effect is solicited. Nonetheless, should any issues remain that might be subject to resolution through a telephonic interview, the Examiner is invited to telephone the undersigned at the numbers provided below.

I hereby certify that this correspondence is being submitted via Electronic Filing System herewith:

Halka Gordon — Nov. 7, 2007

Halka Gordon — Date of Signature

Respectfully submitted,

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